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May 1956

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A TRANSISTOR D-C NEGATIVE IMMITTANCE CONVERTER

by
M. A. Karp

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THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
Silver Spring, Maryland

Operating under Contract NOrd 7386 with the Bureau of Ordnance, Department of the Navy

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A Transistor D-C Negative Immittance Converter

I. INTRODUCTION

In the realization of desirable networks the designer has two quantities at his disposal, resistance and reactance. The latter is considered pure imaginary, but occurs naturally with either sign. Resistance is a real parameter restricted to positive values when passively obtained. To complete the group it is necessary to employ active elements in order to achieve a negative resistance. Various devices that exhibit negative resistance characteristics have long been known. The utilization of these devices has been deterred by their inherently large power consumption. Junction transistors are particularly applicable in this domain due to their ability to produce appreciable amplification while demanding small amounts of power.

A circuit that produces an immittance at its input terminals that is the negative of its load immittance is called a converter. The converters considered will have ground as a reference and respond to d-c voltages. An ideal converter may be defined as, "an active four pole which is completely characterized by two properties: the input

current equals the output current and the input voltage equals the negative of the output voltage."[1] Hence, the ideal converter has a voltage transfer of minus one, a current transfer of unity, and acts like an ideal transformer with a negative input immittance. The circuits described are similar to those suggested by Linvill[2] with one important difference. Due to the fact that there are two basic kinds of transistors, NPN and PNP, one may cascade transistors without resorting to coupling condensers. This fact is used with the result that a zero frequency converter is obtained consisting of two transistors and four resistors.

Negative resistances may be obtained in a variety of ways. One specific configuration that converts a passive load to its negative is described using the small signal equivalent circuit to obtain various limiting conditions imposed upon the transistor and the frequencies of conversion. Equations are derived to permit the design of a specific converter. Due to the direct coupling the question of temperature sensitivity is discussed. One obvious use of a negative immittance is in oscillator circuits. Oscillators are excluded from this paper, but the question of

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[1] J. G. Linvill, "Transistor Negative Impedance Converters," Proc. I.R.E., Vol. 41, pp 725-729, June 1953

[2] J. G. Linvill, "RC Active Filters," Proc. I.R.E., Vol. 42, pp 555-564, March 1954.

stability is dealt with. Finally, laboratory data is presented to substantiate the analytical work.

II. GENERAL

Before deriving the equations for a specific circuit, consideration of what is required of a device if it is to produce a negative immittance is appropriate. This is most conveniently done using the basic theorem presented by Bode[3].

The impedance measured between any two terminals in a mesh of an active circuit is:

$$Z = Zo \frac{F(o)}{F(\infty)} \tag{1}$$

where

Zo = The impedance that would be measured if the active element was zero; that is, the passive mesh impedance.

F(o) = One minus the loop gain with the terminals in question shorted; that is, Δ/Δ° with the circuit in its normal condition*.

[3] H. W. Bode, "Network Analysis and Feedback Amplifier Design," p. 67, D. Van Nostrand Co., 1945.

*Δ° is the determinant of the circuit with the active element set equal to zero.

$F(\infty)$ = One minus the loop gain with the terminals in question opened; that is, Δ/Δ° with the self impedance in the mesh made equal to infinity.

From equation (1) it is obvious that gain must be supplied. To provide a pure negative resistance, with Zo resistive, $F(o)$ and $F(\infty)$ must be of opposite sign, but a negative resistance will be obtained whenever $F(o)$ and $F(\infty)$ are separated by at least 90°, but not more than 270°. Therefore, the necessary conditions for Z to contain a negative real part are:

a. The device must contain active elements.

b. The arg $(F(o)/F(\infty))$ must be more than $\pi/2$, but less than $3\pi/2$.

Consistent with all useful active devices, the previous two conditions must result in a stable impedance.* It will be shown in Section VIII that this means that the net resistance must be positive to ensure stability. These three conditions are necessary and sufficient for a device to produce a stable negative impedance.

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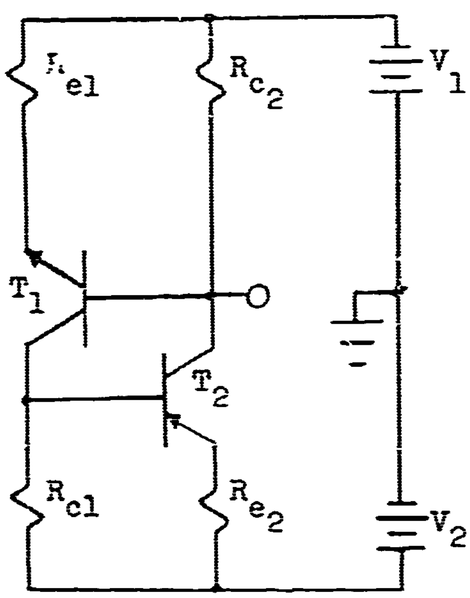
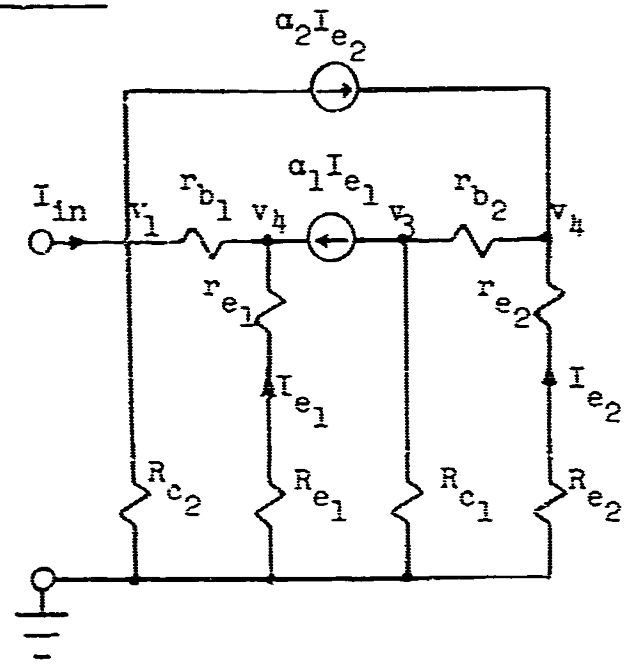
*As previously stated, oscillators are not considered in this investigation.

The final condition uncovers a major distinction between positive and negative resistances. Whereas in passive circuit design the stability of a circuit is independent of the source, the stability of a negative resistance device is intimately related to the source. This fact requires that a negative immittance must be driven from the proper generator to describe its operation. No such restriction is necessary when describing passive immittances. It is also possible for a negative resistance to act differently depending upon its past history. The section devoted to stability will deal more fully with this subject.

III. SHORT CIRCUIT STABLE CONVERTER





Figures 1(a) and (b)
Unbalanced Short Circuit Stable D-C Converter
Schematic and A-C Equivalent Circuit

The circuit of Figure 1(a) is very similar to the familiar multivibrator. It is seen that the transistors are properly biased, due to the NPN-PNP** connection. The driving point admittance to node one will be developed since it is later shown that this is a short circuit stable configuration, i.e., I/E has no RHP poles. It is assumed that a current, I_{in}, exists as shown but one should not infer that a current generator will be the driving force. The transistor collector impedance, Z_c, is much larger than any external load, and is therefore neglected.

The small signal, low frequency nodal equations for the circuit of Figure 1(b) are:

$$\begin{bmatrix} I_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} (G_{c_2} + g_{b_1}) & -g_{b_1} & 0 & \alpha_2 G_2 \\ -g_{b_1} & (g_{b_1} + (1-\alpha_1)G_1) & 0 & 0 \\ 0 & \alpha_1 G_1 & (g_{b_2} + G_{c_1}) & -g_{b_2} \\ 0 & 0 & -g_{b_2} & (g_{b_2} + (1-\alpha_2)G_2) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix}$$

** This simple configuration cannot be duplicated using vacuum tubes due to the fact that the only means of current transportation in a vacuum tube is by electron flow.

Where

$$G_1 = \frac{1}{r_{e_1} + R_{e_2}}, \quad G_2 = \frac{1}{r_{e_2} + R_{e_2}}$$

The input admittance, Y_{in}, is obtained from:

$$Y_{in} = Y_o \frac{F(\text{with terminal (1) to gnd open})}{F(\text{with terminal (1) to gnd shorted})} = Y_o \frac{F(o)}{F(\infty)}$$

Y_o may be obtained from the equation as $\Delta^\circ/\Delta^\circ_{11}$, or from the circuit by inspection as:

$$Y_o = G_{c_2} + \frac{g_{b_1} G_1}{g_{b_1} + G_1} \approx G_{c_2} + G_1 \text{ for } g_{b_1} >> G_1$$

$$F(o) = \frac{\Delta}{\Delta^\circ} \approx \frac{(G_{c_2} G_{c_1} - \alpha_1 \alpha_2 G_1 G_2)}{(G_{c_1} + G_2)(G_{c_2} + G_1)}$$

for

$$g_{b_1} \text{ and } g_{b_2} >> G_{c_1},\ G_{c_2}, \text{ or } G_2.$$

$$F(\infty) = \left.\frac{\Delta}{\Delta^\circ}\right|_{G_{c_2} = \infty} = \frac{G_{c_1}}{G_{c_2} + G_2}.$$

Finally:

$$Y_{in} = G_{c_2} - \frac{\alpha_1\alpha_2 G_1 G_2}{G_{c_1}} \qquad (2)$$

A restatement of the assumptions made in arriving at equation (2) indicates the relation between transistor parameter and external values.

a) α_1 and $\alpha_2 \approx 1$

b) $g_{b_1} \gg G_1$ and $g_{b_2} \gg G_2$

c) $g_{c_1} \ll G_{c_1}$ and $g_{c_2} \ll G_{c_2}$

At this stage the device is not a converter, since the output terminal has not been designated. Choosing emitter one as the output with $G_2 = G_{c_1} = G_{c_2} = G$ and $G_1 = G + G_x$ equation (2) may be rewritten as:

$$Y_{in} = G(1-\alpha_1\alpha_2) - \alpha_1\alpha_2 G_x \approx -\alpha_1\alpha_2 G_x \text{ , for } G_x \approx G \qquad (3)$$

Therefore, the circuit produces a linear* conversion of load conductance, G_x, to its negative at the input. Although the linearity is not necessary, it obviously enhances the

*Linear conversion is used here to indicate the straight line relationship between Y_{in} and G_x. It should not be confused with linearity of the I/E characteristics.

utility of the device and is therefore desirable. Since the a-c circuit is symmetrical either collector base junction may be chosen as the input and either emitter as the output. Investigation of the d-c characteristics will show that the d-c operation will vary depending upon the choice of input and output terminals. A circuit diagram of the admittance converter is shown in Figure 2.

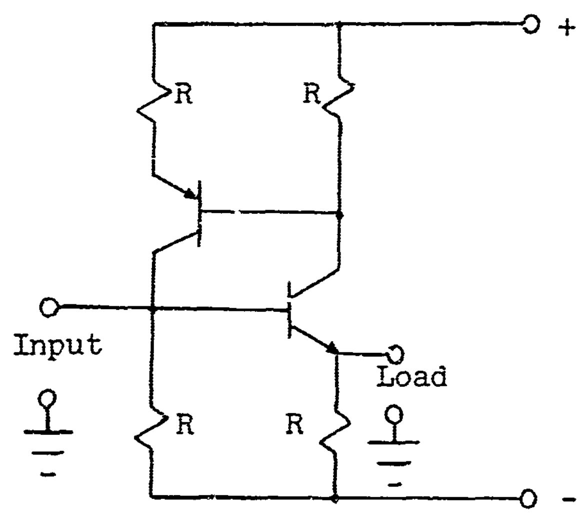


Figure 2. Short Circuit Stable Converter Circuit Diagram

IV. OPEN CIRCUIT STABLE CONVERTER

Section III has shown that the input admittance at either collector will be the negative of the load admittance at either emitter. Let us now consider the

input impedance at either emitter with a load on either collector. The impedance is considered in this case due to the fact that it will be shown that this configuration is open circuit stable, i.e., E/I has no RHP poles. Referring to Figure 1(b) the input impedance to node two, or four, will be derived. Although node two is not a physically accessible point it is at a voltage very near the junction of the internal emitter resistance, r_e, and the external emitter resistor R_e.

Since the admittance matrix is not a function of the generator position, the equations of the short circuit stable converter are still valid in connection with the open circuit stable converter. F(o) is measured with the circuit in its normal condition, and, therefore, it is unchanged. With the active generator equal to zero the impedance from node two to ground is essentially equal to that of node one to ground. Since node two is not the physical input it is important in calculating $F(\infty)$ to remember that

$$G_1 = \frac{1}{R_{e_1} + r_{e_1}} \approx \frac{1}{R_{e_1}} ,$$

does not go to zero but approaches g_{e_1}. With this in mind the input impedance to node two is arrived at, as shown in Appendix "A" as:

$$Z = -\alpha_1\alpha_2R_x \qquad (4)$$

where R_x is an impedance connected in parallel with R_{c_2}, and emitter one is the input terminal. As for the short circuit stable converter, the circuit is symmetrical a-c-wise but not d-c-wise. Figure 3 is a circuit diagram of the open circuit stable converter.

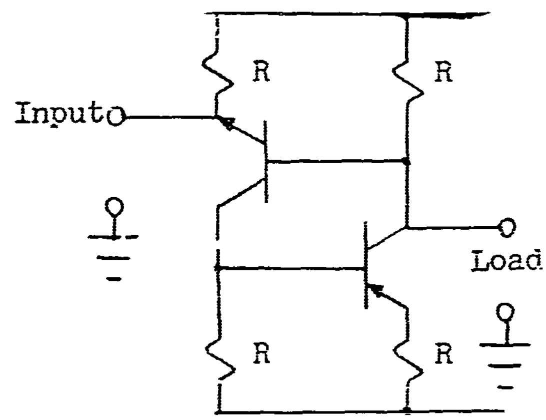


Figure 3. Open Circuit Stable Converter Circuit Diagram

V. DESIGN EQUATIONS

The design of active devices is often reduced to an equivalent circuit that permits the choice of various parameters so as to produce a final circuit meeting the desired operating specifications. This reduction assumes that the active element is always operating in its linear region. Equations (3) and (4) have been derived with this assumption in mind. When the input generator is of such a magnitude so as to back bias the emitter-base junction or forward bias the collector-base junction, these equations will no

longer properly describe the operation of the converter.

It is desirable to have an analytical expression for the end points of the linear region. This expression might be of the form, $E = rI + v$, where r and v are functions of E. An alternative method is to partition the over-all characteristic into regions whereby an expression is obtained for each region and the intersections of the appropriate expressions determine the crossover points. The advantage of this method is that each of the three equations is linear and the techniques of linear circuit analysis are applicable.

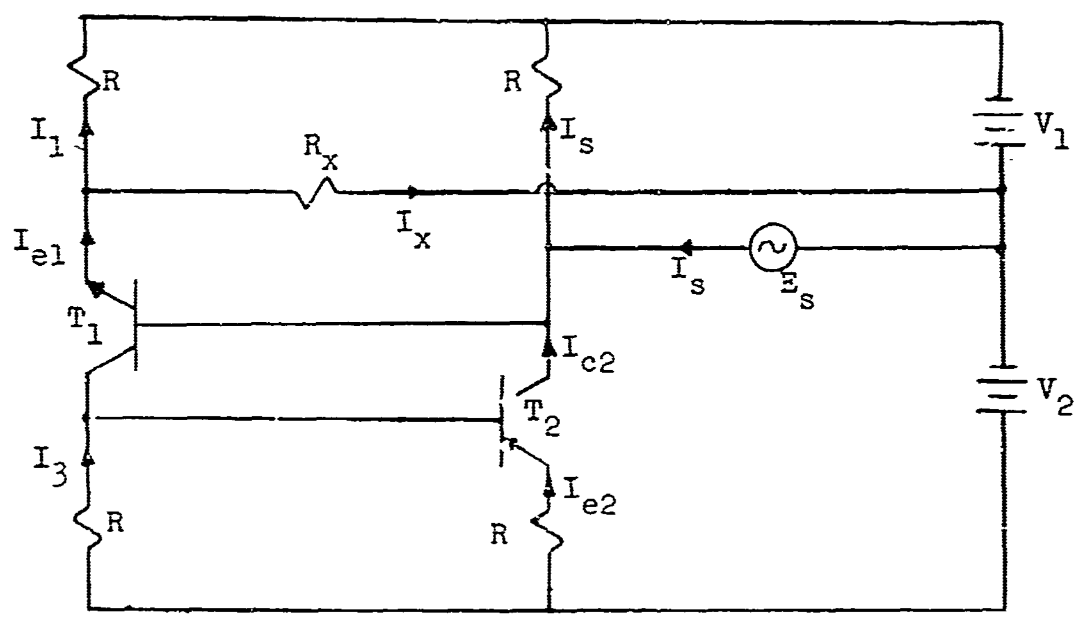


Figure 4. Short Circuit Stable Converter, Active Region

Figure 4 indicates the converter with both transistors operating in their active region. This region is defined by:

V_{be} = constant and $\alpha_1 \approx \alpha_2 \approx 1$.

With these definitions in mind the currents are:

$$I_1 = \frac{E_s + V_1 - V_{be_1}}{R} \; , \; I_2 = \frac{E_s + V_1}{R} \; , \; I_x = \frac{E_s - V_{be_1}}{R_x} \; .$$

Since $I_{b1} \approx I_{b2} \approx 0$,

$$I_3 = I_{c1} = I_{e1} = \alpha_1(I_1 + I_x) = I_{e2} - \frac{V_{be_2}}{R} \; ,$$

$$I_s = I_2 - I_{c2} = I_2 - \alpha_1\alpha_2(I_1 + I_x) + \alpha_2 \frac{V_{be_2}}{R} \; .$$

Substituting for the currents in terms of the known source and supply voltages, the following results:

$$I_s = -G_xE_s + V_{be}[2G + G_x] \tag{8}$$

This result differs from equation (3) due to the fact that the a-c equivalent circuit analysis assumed $V_{be} = 0$.

When the input voltage is negative and approximately equal to V_1, the emitter current of T_1 becomes zero. The boundary between the active and cutoff regions is defined by $I_{e1} = 0$. This results in the simple one mesh circuit of E_s plus R in series with V_1. Hence:

$$I_s = E_sG + V_1G \tag{9}$$

is the proper equation for the converter in the cutoff region. Since T_1 is cut off only I_{co} flows in its collector and, therefore, T_2 is also cut off due to having both its emitter and base returned to the same voltage.

The final region is reached when E_s is made positive enough so that the collector-base voltage is zero. The boundary between the active and saturation regions is defined by $V_{cb} = 0$. When this occurs the collector joins the base and emitter, which have been following each other, and the three terminals degenerate to one. This results in two forward biased junctions with an equivalent circuit as shown in Figure 5(a).

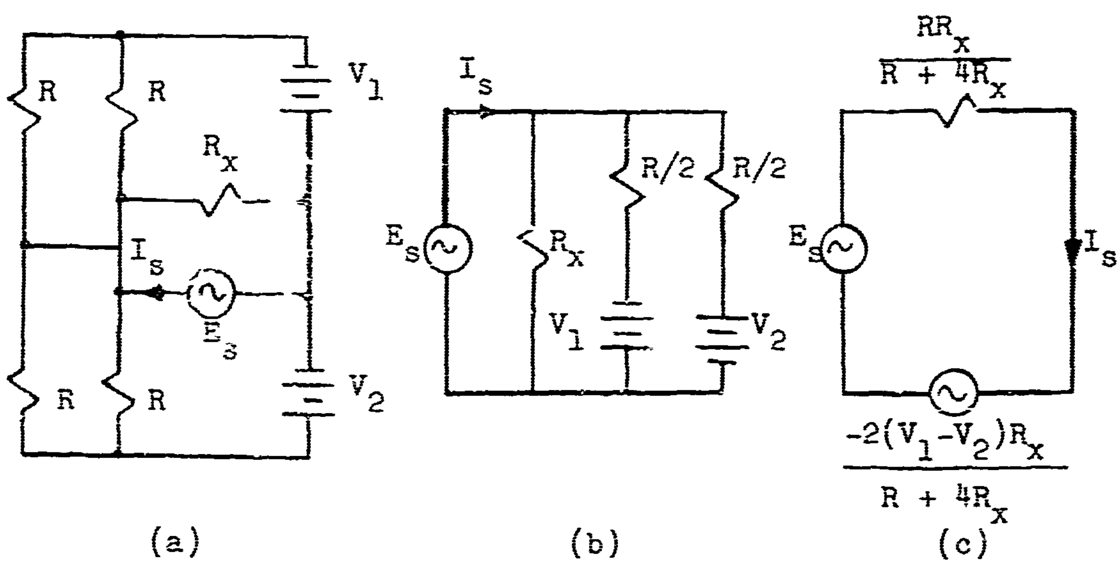


Figure 5. Short Circuit Stable Converter Saturation Region

Figures 5(b) and 5(c) are Thevinin equivalents of (a) and (b) respectively. Hence, the following equation is valid

in the saturation region:

$$I_s = (4G + G_x)E_s + 2G(V_1 - V_2) \tag{10}$$

Equations (8), (9), and (10) describe the complete characteristics of the short circuit stable converter. It is seen that only equation (8), the active region, contains a negative slope. The V and I intercepts of this slope are independent of the supply voltage, but are determined by the transistor emitter-base voltage drop. The slope in the cutoff region is independent of G_x, whereas the slope in the saturation region is a function of the conductance to be converter. Both cutoff and saturation curves have V and I intercepts that are functions of the supply voltages.

Each of the three equations is linear, and, therefore, the intersection of any two determines the coordinates of points that have been termed peak and valley points. Proper choice of supply voltages and bias resistors permits the designer to build a specified short circuit stable converter that will operate linearly for a known input swing. Equating (8) and (9) results in the coordinates of the peak point:

$$E_s = \frac{-V_1 + (2 + R/R_x)V_{be}}{1 + R/R_x}$$

$$I_s = \frac{V_1 + (2R_x/R + L)V_{be}}{R + R_x} \tag{11}$$

Equating (8) and (10) the valley point is obtained as:

$$
\begin{aligned}
E_s &= \frac{(V_1 - V_2)}{2 + R/R_x} + \frac{V_{be}}{2} \\
I_s &= \frac{V_1 - V_2}{R + 2R_x} + \frac{V_{be}}{2} \left(\frac{R + 4R_x}{RR_x}\right)
\end{aligned}
\qquad (12)
$$

In calculating these points the small voltage, V_{be}, is assumed equal for both transistors and $\alpha_1\alpha_2$ is made equal to unity. Interchanging load and generator, plus substituting a current generator for the voltage generator, results in the open circuit stable converter shown in Figure 6.

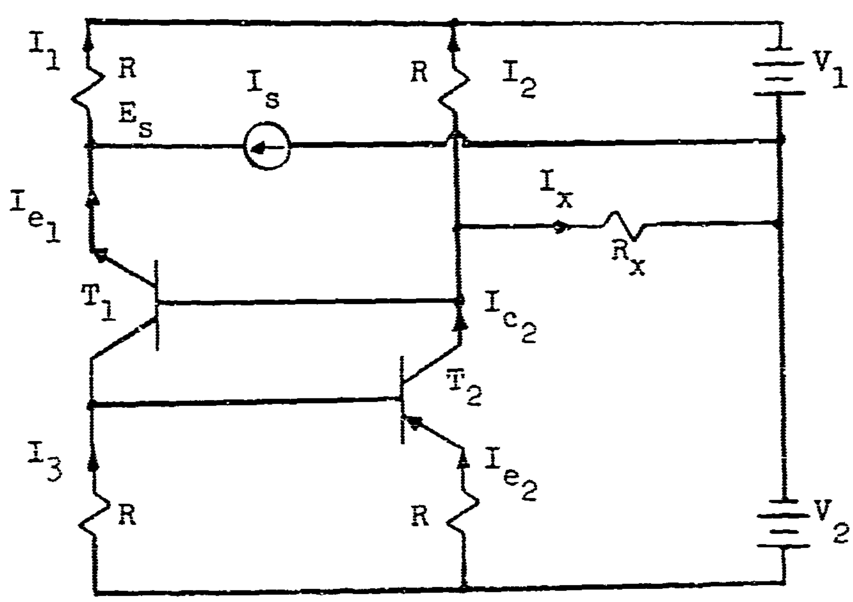


Figure 6. Open Circuit Stable Converter Active Region

This change, plus the fact that the previously derived equations are linear, permits one to use the principle of duality to obtain the equations for the open circuit stable converter. This results in:

$$\text{Active} \qquad E_s = -R_x I_s - V_{be}(2\ R_x/R + 1) \tag{13}$$

$$\text{Cutoff} \qquad E_s = RI_s - V_1 \tag{14}$$

$$\text{Saturation} \qquad E_s = \frac{RR_x I_s}{R + 4R_x} - \frac{2R_x}{R + 4R_x}(V_1 - V_2) \tag{15}$$

These equations may be obtained by solving equations (8), (9), and (10) for E_s as a function of I_s. The coordinates of the peak and valley points are unchanged. Due to the change of input point, and source, the polarity that saturates short circuit stable converter cuts off open circuit stable converter.

Whereas the a-c equivalent circuit is symmetrical, Figures 4 and 6 indicate that the complete characteristics are quite different when R_x is connected to different emitters. The equations for both converters, with R_x connected to T_2 may be derived in the same manner as has been shown.

VI. FREQUENCY RESPONSE

The equations previously derived indicate th-t the input immittance is the negative of the load immittance. This will be true for a restricted range of frequencies. Due t-

the fact that the collector impedance has been neglected and no frequency characteristic has been associated with α, these equations are valid only at frequencies less than ω_o, the α cutoff frequency of the transistor.

To investigate the frequency response of the short circuit stable converter the equivalent circuit of Figure 7(b) is used. This two-node circuit is a reduction of Figure 7(a) with the assumption that r_e and r_b are negligible and that y_c, the collector admittance, is now pertinent.

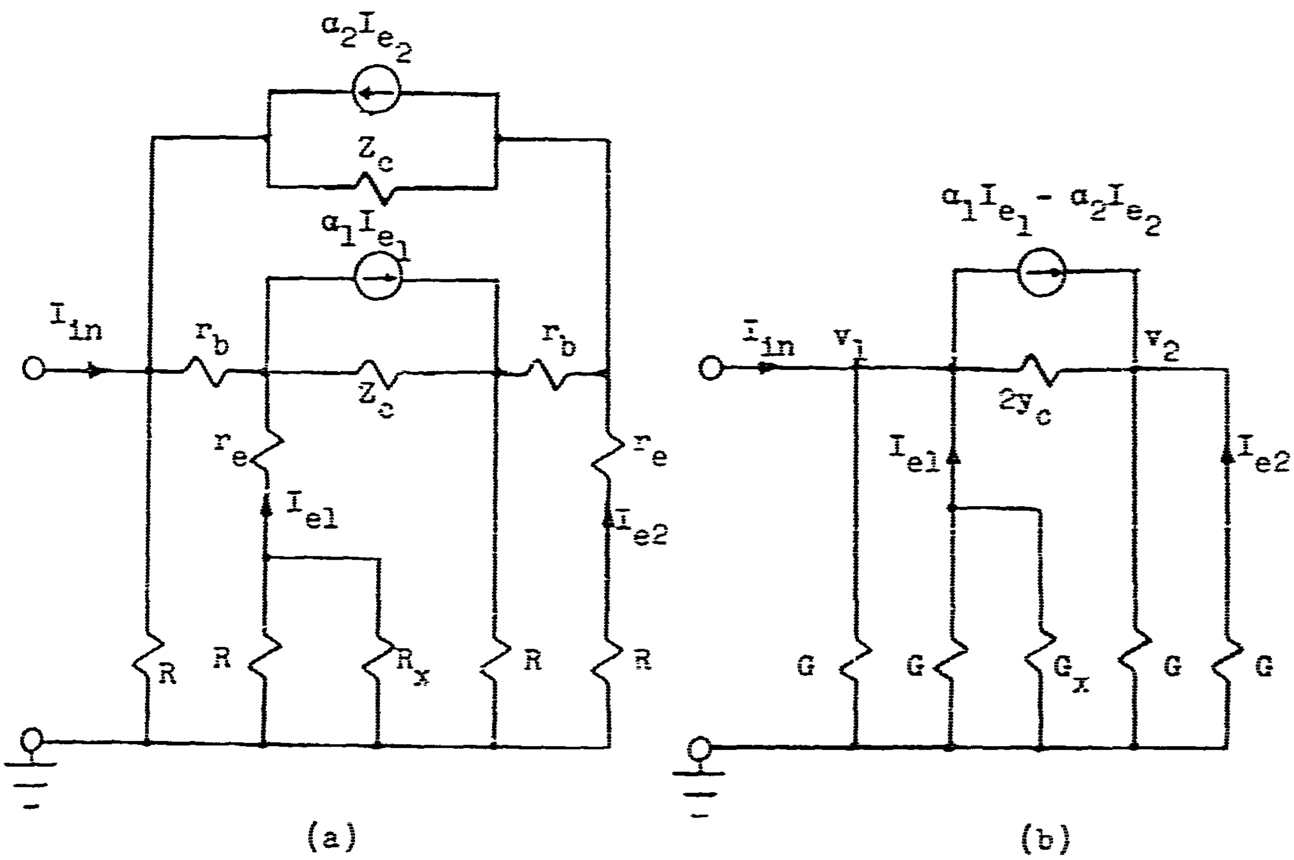


Figure 7. Short Circuit Stable Converter and Reduced Equivalent Circuit

The equations that describe this circuit are:

$$\begin{bmatrix} I_{in} \\ \\ 0 \end{bmatrix} = \begin{bmatrix} G(2 - \alpha_1) + G_x(1 - \alpha_1) + 2y_c & -(2y_c - \alpha_2 G) \\ \\ -(2y_c - \alpha_1[G + G_x]) & G(2 - \alpha_2) + 2y_c \end{bmatrix} \begin{bmatrix} V_1 \\ \\ V_2 \end{bmatrix}$$

Since $Y_{in} = \Delta/\Delta_{11}$ it is necessary to obtain Δ and Δ_{11}.

$$\Delta = 2G^2(2 - \alpha_1 - \alpha_2) \quad G[8y_c + G_x(2 - 2\alpha_1 - \alpha_2)] + 2y_c G_x$$

$$\Delta_{11} = G(2 - \alpha_1) + 2y_c$$

Let $\alpha_1 \approx \alpha_{o1}(1 - pT_1)$ where $T_1 = \dfrac{1}{\omega_{o1}}$

$\alpha_2 \approx \alpha_{o2}(1 - pT_2)$ $T_2 = \dfrac{1}{\omega_{o2}}$

Therefore:

$$Y_{in} = \frac{-GG_x + 2G_x y_c + 8Gy_c + p(G_x + 2G)G(T_1 + T_2)}{G + 2y_c + pT_2 G}$$

substituting:

$$y_c = g + pC$$

$$Y_{in} \approx \frac{-G_x + p(GK_1 + 2CK)}{1 + p(T_2 + 2RC)} = \frac{-G_x + pA}{1 + pB} \tag{16}$$

where:

$$K = 4 + R/R_x, \text{ and } K_1 = (2 + R/R_x)(T_1 + T_2).$$

Hence, the input admittance acts like a conductance in parallel with a condenser.

The conductance will be negative until the $R_e(Y_{in}) = 0$. The frequency at which this occurs may be found by setting the real part of equation (16) equal to zero. Doing this one obtains the following:

$$\omega_o^2 = \frac{G_x}{(T_2 + 2RC)(GK_1 + 2CK)} = \frac{C}{AB} \tag{17}$$

A second significant frequency may be defined as the 3 db point of admittance. This frequency may be found as follows:

$$Y_{in} = \frac{-G_x + pA}{1 + pB} = \frac{-G_x + \omega^2 AB + j\omega(A + BG_x)}{1 + \omega^2 B^2}$$

$$R_e Y_{in}(\omega) = \frac{-G_x + \omega^2 AB}{1 + \omega^2 B^2}$$

$$Y_{in}(o) = -G_x$$

$$R_e Y_{in}(\omega_{3db}) = -\frac{G_x}{\sqrt{2}} = \frac{-G_x + \omega^2 AB}{1 + \omega^2 B^2},$$

therefore,

$$\omega_{3db} = \frac{.414G_x}{B(\sqrt{2}\,A + BG_x)} = \frac{.414\omega_o^{\,2}}{2 + (\omega_o B)^2}$$

This frequency may be taken as a design criterion analogous to 3 db bandwidth as used in amplifier design. Given a transistor with a known α cutoff frequency and collector capacity, a prescribed negative conductance may be obtained up to a specified frequency by properly choosing R. Naturally high α cutoff and low capacity are desirable in obtaining high frequency operation.

The input impedance of the open circuit stable converter is derived completely in Appendix B. The results are as follows:

$$Z_{in} = R_x \frac{-1 + p(2RC + T_2 + 2T_1)}{1 + p(2CK + GK_1 - T_1G_x)R_x} = R_x \frac{-1 + pA'}{1 + pB'}$$

Therefore, the input impedance acts like a resistance in series with an inductance. This resistance will be negative until $R_e(Z_{in}) = 0$. Therefore,

$$\omega_o^{\,2} = \frac{G_x}{(2RC + T_2 + 2T_1)(2CK + GK_1 - T_1G_x)} = \frac{G_x}{A'B'}$$

As was done for the short circuit stable converter a 3 db of impedance may be computed as:

$$\omega_{3db} = \frac{.414}{B'(\sqrt{2}A' + B')} = \frac{.414\omega_o^2}{\sqrt{2} + (B'\omega_o)^2}$$

These equations indicate the relationship between the open circuit stable converter input impedance and frequency have the same form as the short circuit stable converter input admittance with a small change in ω_o and ω_{3db}. The section devoted to experimental results shows that for equal loads, using the same circuit, these differences are imperceptible. The results of this section indicate the frequency dependency of both converters and the equations developed may be used if the designer is interested in frequencies above the audio range.

VII. TEMPERATURE EFFECTS

A discussion of the capabilities of a device that includes transistors is not complete without exploring the important question of temperature. Although all transistor parameters are a function of temperature, (this is due to the ever present factor KT/q), experience has shown that I_{co}, α, and r_e are the most sensitive in direct coupled amplifier design.

I_{co} is the reverse collector saturation current that is exponentially related to temperature. With the emitter of a transistor open, so that only I_{co} flows in the collector-base junction, this current will double with every 8°C increase in temperature. Shea[4] has shown that a bias stability factor, S_B, may be developed to determine the change of collector current as a function of a change in I_{co}.

$$S_B = \frac{\partial I_c}{\partial I_{co}} = \frac{R_e + R_b}{R_e + R_b(1-\alpha)}$$

R_b = Effective resistance from base to grou.d.

R_e = Effective resistance from emitter to ground.

This relationship assumes that α is constant over the temperature range. For the open circuit stable converter the bias stability of T_2 is:

$$S_2 = \frac{R_e + R_c}{R_e + R_c(1-\alpha)} = \frac{2}{2 - \alpha_2} = 2 \; .$$

For T_1:

$$S_1 = \frac{R_e + R_c R_x/R_c + R_x}{R_e + R_c R_x/R_c + R_x(1-\alpha_1)} = \frac{2R_x + R}{R + R_x(2-\alpha_1)} \approx \begin{cases} 2 \text{ for } R_x \rightarrow \infty \\ 1 \text{ for } R_x \rightarrow 0 \end{cases}$$

---

[4] R. F. Shea, "Principles of Transistor Circuits," John Wiley and Sons.

Therefore, a one microampere change in I_{co} will produce twice as much change in the collector current of each transistor, in the worst case. Some question may have come up regarding the necessity of having the resistors in each collector. The removal of these resistors would make the device extremely temperature sensitive, as the equation for S_B indicates. R_b would become the output resistance of the transistor and the bias stability would approach $1/1-\alpha$.

For the short circuit stable converter the same equations are valid, but since the source is one of very low internal resistance (a voltage generator) this resistance must be included in the calculation of S_B.

The internal emitter resistance, r_e, is approximately equal to $\frac{KT/q}{I_e}$*. This causes the input resistance of a transistor to vary with temperature. Any external emitter resistance will reduce the effect of this variation. Since $r_e \approx 26\Omega$, at 1 ma emitter current, it is simple to swamp out the change of r_e in either converter.

If either α were to change substantially the assumption made in arriving at equations (3) and (4) may become invalid. Experiment has shown that the α of a germanium transistor does not change radically, but if this is an important factor then one may resort to a compound

---

*This approximation neglects the small quantity I_{co}.

transistor as suggested by Darlington.

VIII. STABILITY

Although the term negative resistance implies an element that behaves in the opposite sense of a positive resistance, this is only partially true. As has been shown, a device has a negative immittance for a limited range of input levels. More important than this distinction is the fact that a negative immittance device is only stable with proper terminations.

Any circuit may be characterized by its pole-zero distribution in the complex frequency plane. Investigating passive driving point immittances one discovers that there are no right half plane poles or zeros, and the passive circuit is unconditionally stable. Hence, one might intuitively say that if an active circuit has no right half plane poles or zeros, it too is unconditionally stable. Let us consider any network, for which we desire one particular variable i_n or e_n. If the network has only one impressed source e_n or i_n, then,

$$\Delta i_n = \Delta_{nn} e_n,$$

where Δ is the determinant of the impedance matrix, and Δ_{nn} is the determinant with the n^{th} row and n^{th} column deleted.

Using $p = \sigma + j\omega$, both Δ and Δ_{nn} are polynomials in p. If the source is a voltage and we desire the transient solution then,

$$(a_s p^s + a_{s-1} p^{s-1} + \text{-------} 1) i_n = 0$$

must be solved. If the source is a current then,

$$(a_r p^r + a_{r-1} p^{r-1} + \text{-------} 1) e_n = 0$$

must be solved. Using the first equation as an example, to investigate the conditions for stability we first factor as follows:

$$[(p-p_1)(p-p_3) \text{-------}) i_n = 0$$

Then the solution, assuming simple roots, is

$$i_n = A_1 e^{p_1 t} + A_2 e^{p_2 t} + \text{-------}$$

Using one term of the above we find the following possible solutions for i_n:

a) $i_n = A_1 e^{\pm\sigma_1 t}$

b) $i_n = e^{\pm\sigma_1 t}(A_1 e^{j\omega_1 t} + A_2 e^{-j\omega_1 t})$

c) $i_n = A_1 e^{j\omega_1 t} + A_2 e^{-j\omega_1 t}$

It is apparent that any solution involving a positive σ ultimately will result in an infinite response. Hence, it is clear that the condition for stability is that the root p_1 must lie in the left half plane. Since p_1 is a root of Δ we can conclude that the poles of $\Delta_{nn}/\Delta = i_n/e_n$ must lie in the left half of the complex plane for the network to be stable. Similarly, we would have concluded that the poles of $\Delta/\Delta_{nn} = e_n/I_n$ must lie in the left half plane if we had started with a current source.

Let us now consider what circuit elements will produce right half plane poles. It has been stated that any combination of RLC is stable. Therefore, it is clear that only a negative resistance, or conductance, will move σ from the left to the right half plane. We can then state that if a negative resistance, R_n, is fed from a generator, whose source resistance, R_s, is of greater magnitude than R_n, the circuit is stable. Hence, if a negative resistance is fed from a current generator ($R_s \rightarrow \infty$) an unconditionally stable device results. An alternative explanation of this results when one considers a circuit with a net negative resistance to be a source, rather than a sink. Hence, with a source already present there is no requirement for a drive to produce an output.

From the above, the terms "short circuit" and "open circuit" stable may now be associated with devices that require voltage and current generators, respectively.

The conclusion drawn from the above discussion is that a two-terminal active device plus its terminations must satisfy the same stability conditions as a two-terminal passive network.

A dual discussion results in the fact that a negative conductance should be driven from a voltage generator ($G_s \rightarrow \infty$).

According to Linvill[1] all balanced emitter driven devices are open circuit stable, and all collector driven devices are short circuit stable, with passive coupling and resistive loads as long as $|\alpha| \leqslant 1$, or for passive loads as long as α is real and less than unit. These statements are true for unbalanced devices also. Figure 8 indicates the circuit with a passive three-terminal load.

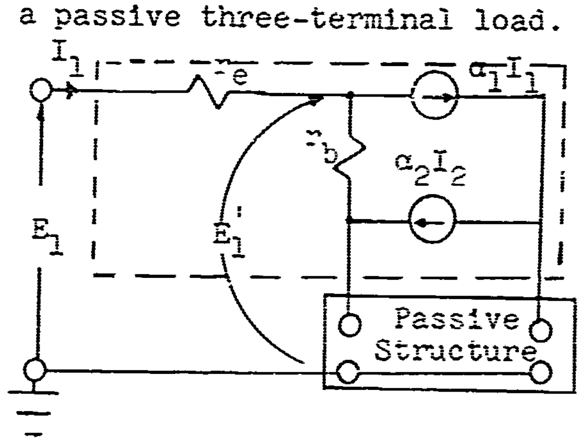


Figure 8. Open Circuit Stable Converter with Arbitrary Cross Coupling

[1] op. cit.

If a device is open circuit stable then:

$$Z_{in} = E_1/I_1,$$

has no right half plane poles. This impedance may be calculated as follows:

$$Z_{in} = r_e + E_1'/I_1 = r_e + (r_b + Z_{11})(1-\alpha_1) + \alpha_1\alpha_2 Z_{12}.$$

Where Z_{11} is the driving point impedance, and Z_{12} the transfer impedance associated with the passive structure. The poles of Z_{in} are the poles of Z_{11}, which are the same as those of Z_{12}. These poles are in the left half plane as required by passive circuitry.

From figure 9 the following may be obtained:

$$Y_{in} = \frac{I_1}{E_1} = \frac{I_{11}}{E_1} = Y_{11} - \frac{\alpha_1\alpha_2}{1 - \alpha_1} Y_{12}.$$

Where Y_{11} is the driving point admittance, and Y_{12} the transfer admittance of the passive structure*. Hence, if α is real and less than 1, Y_{in} has only poles of Y_{11} and Y_{12}, and these poles must lie in the left half plane. This type of converter is therefore short circuit stable.

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*The $1/1-\alpha_1$ is due to the impedance transformation of a grounded collector amplifier.

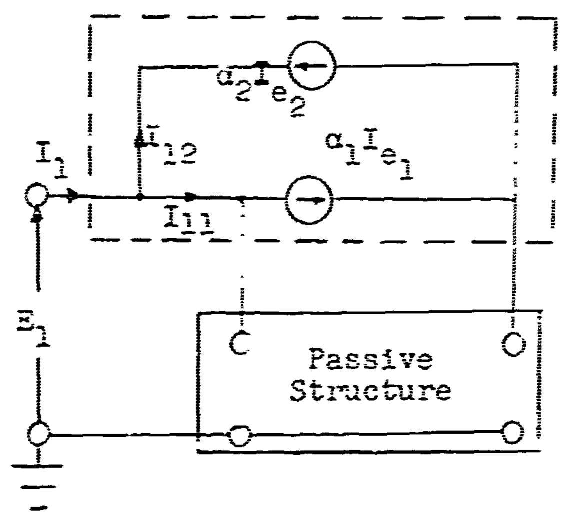


Figure 9. Short Circuit Stable Converter with Arbitrary Cross Coupling

IX. EXPERIMENTAL DATA

In the previous sections various analytical expressions were derived that described the operation of the negative immittance converter. It is appropriate at this time to present the results of several experiments in an attempt to verify these equations. To be more precise, the following data really validates the assumptions made in arriving at the simplified equations.

With the exception of the frequency response curve, all curves were obtained using a Mosley Recorder in the following manner:

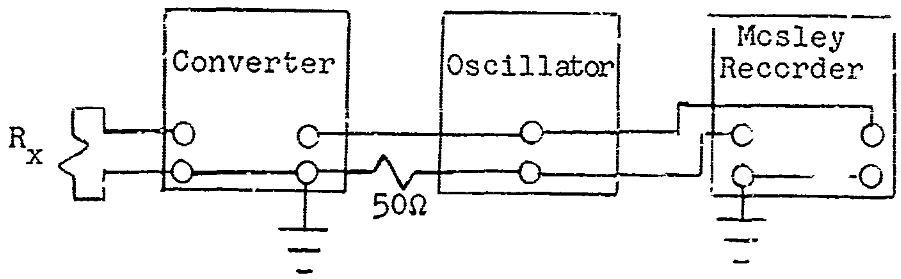


Figure 10. Test Procedure

Hence, the recorder is continuously monitoring the input voltage and input current to the converter. All the data presented utilizes the circuits of Figure 2 or Figure 3 with R = 10K, and transistors that have the following measured parameters:

Transistor	Sylvania 2N35	Sylvania 2N34
$r_c \times 10^6$	3.3	3.3
α	.952	.96
r_b	800	400
r_e	20	50
$I_{co} \times 10^6$	5	1.5
$f_{\alpha co} \times 10^6$	700 kc	900 kc
$C_c \times 1^{-12}$	18	15
Zener Voltage	30	45

Figure 11 indicates the input conductance of the short circuit stable converter as a function of G_x. All curves are forced through the origin to permit easy comparison of slopes. It can be seen that the linearity is extremely good for $G_x > 200\mu v$. The reduced linearity is due to the appearance of the $G(1-\alpha_1\alpha_2)$ term in equation (3). A similar set of curves for the open circuit stable converter as a function of R_x is shown in Figure 12. The linearity in this case is reduced when $R_x(\alpha_1\alpha_2 - 1)$ becomes significant with respect to R. The tables below compare the measured and calculated values for both converters.

G_x	800	400	200	100	50	μ ℧
Measured $-G_{in}$	720	360	178	83.0	35.4	μ ℧
Calculated $-G_{in}$	725	364	182	91.0	45.5	μ ℧

R_x	1.25	2.5	5K	10K	20K	KΩ
Measured $-R_{in}$	1.10	2.30	4.35	8.30	16	KΩ
Calculated $-R_{in}$	1.13	2.26	4.55	9.05	18.1	KΩ

Figure 13 is a plot indicating the complete characteristics of the short circuit stable converter. The curves show the peak and valley points plus voltage and current bias as a function of G_x. Figure 14 is a plot of the open circuit stable converter complete characteristics

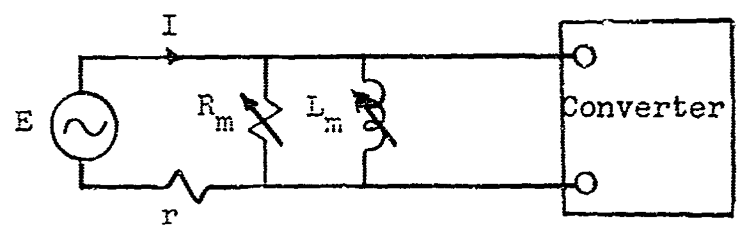
Figures 15 and 16 are presented to show the comparison between an experimental curve and a curve plotted using the equations derived for each linear region. These curves also indicate that the peak and valley coordinates may be correctly computed.

Although no attempt has been made to analytically consider distortion, it was felt that some data should be presented indicating the magnitude of the distortion in the active region. Using a one kilocycle signal, wave analyzer measurements showed that the total harmonic distortion was at all times less than one per cent.

Figures 17 and 18 show the effect an increase in temperature has on the short circuit and open circuit stable converters, respectively. There is no perceptible change in slope and, therefore, point by point measurements were made at 28° and 72°C. These showed a three per cent change in the open circuit stable converter but none in the short circuit stable converter. The recordings do, however, indicate a radical change in peak, valley, and bias points. These changes are due to the dependency of I_{co} and V_{eb} with temperature. The design equation should be amended to include these effects if they are of importance. As they stand I_{co} is neglected and V_{eb} is assumed small and constant. This d-c shift is inherent

to the direct connection and must be considered in the design of a converter that must operate over an extended temperature range.

The equation given for the admittance of the converter as a function of frequency may be verified using the following circuit :



By varying R_m and L_m a voltage null is obtained across r. This may be seen as follows:

$$Y_m = G_m + \frac{1}{pL_m}, \qquad Y_x = -G_x + pc_x .$$

Therefore,

$$Y_{total} = (G_m - G_x) + pc_x + \frac{1}{pL_m}$$

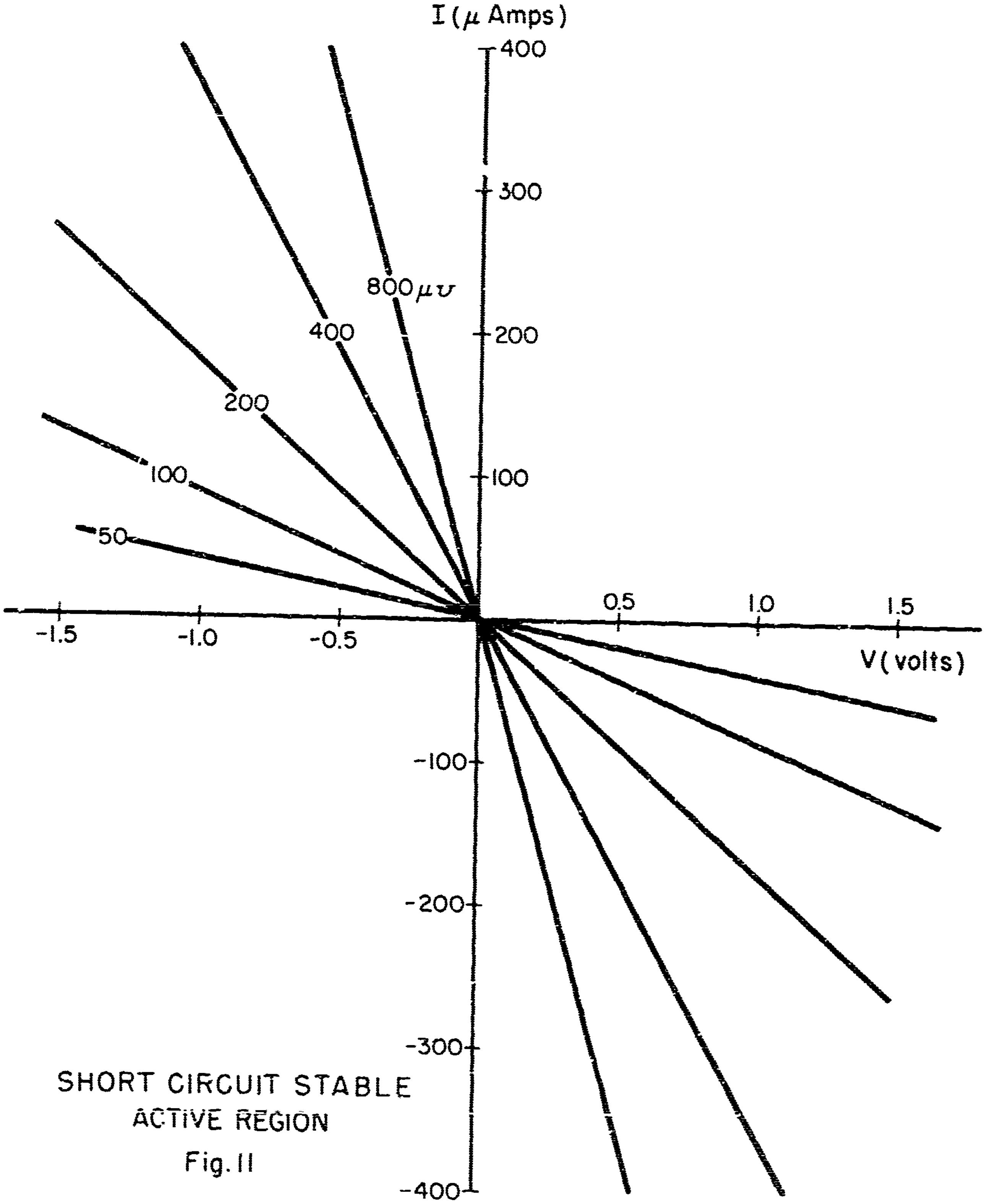
$$I = EY_T = [\ (G_m - G_x) + \frac{p^2L_mC_x + 1}{pL_m}]E$$

$$I_r = [\ (G_m - G_x) + \frac{1 - \omega^2L_mC_x}{jL_m}$$

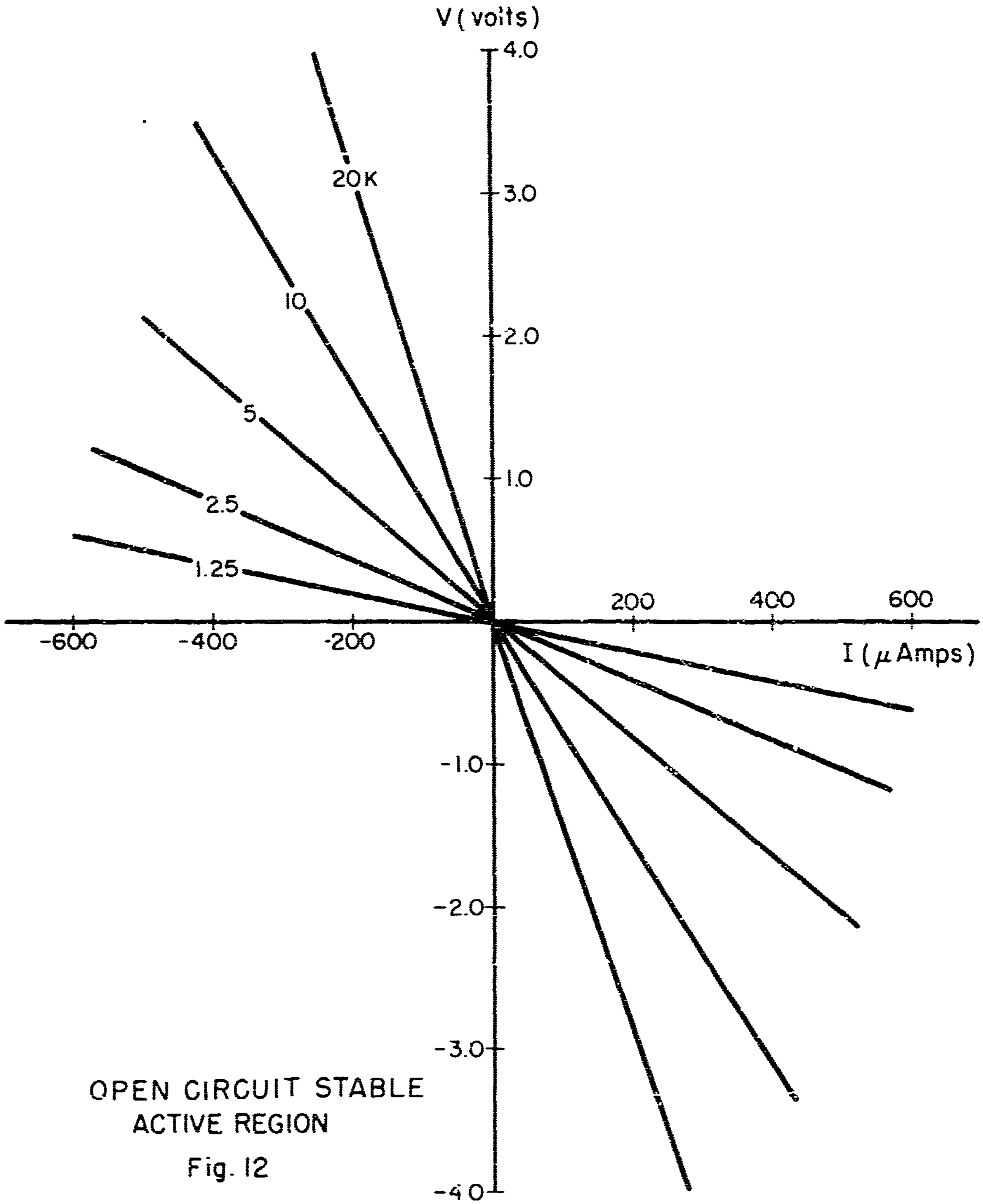
Hence, at $\omega^2 L_m C_x = 1$, and $G_m = G_x$, the voltage across r is equal to zero. By recording G_m and L_m as a function of ω the admittance as ω varies may be plotted as shown in Figure 19.

The fact that the locus of Y versus ω encloses the origin in a clockwise sense is another indication of the short circuit stability of the device. Changing the real axis from G, in micromhos, to R, in KΩ, produces the locus of Z_{in} versus ω. In this case open circuit stability is indicated by the clockwise encirclement of the origin*.

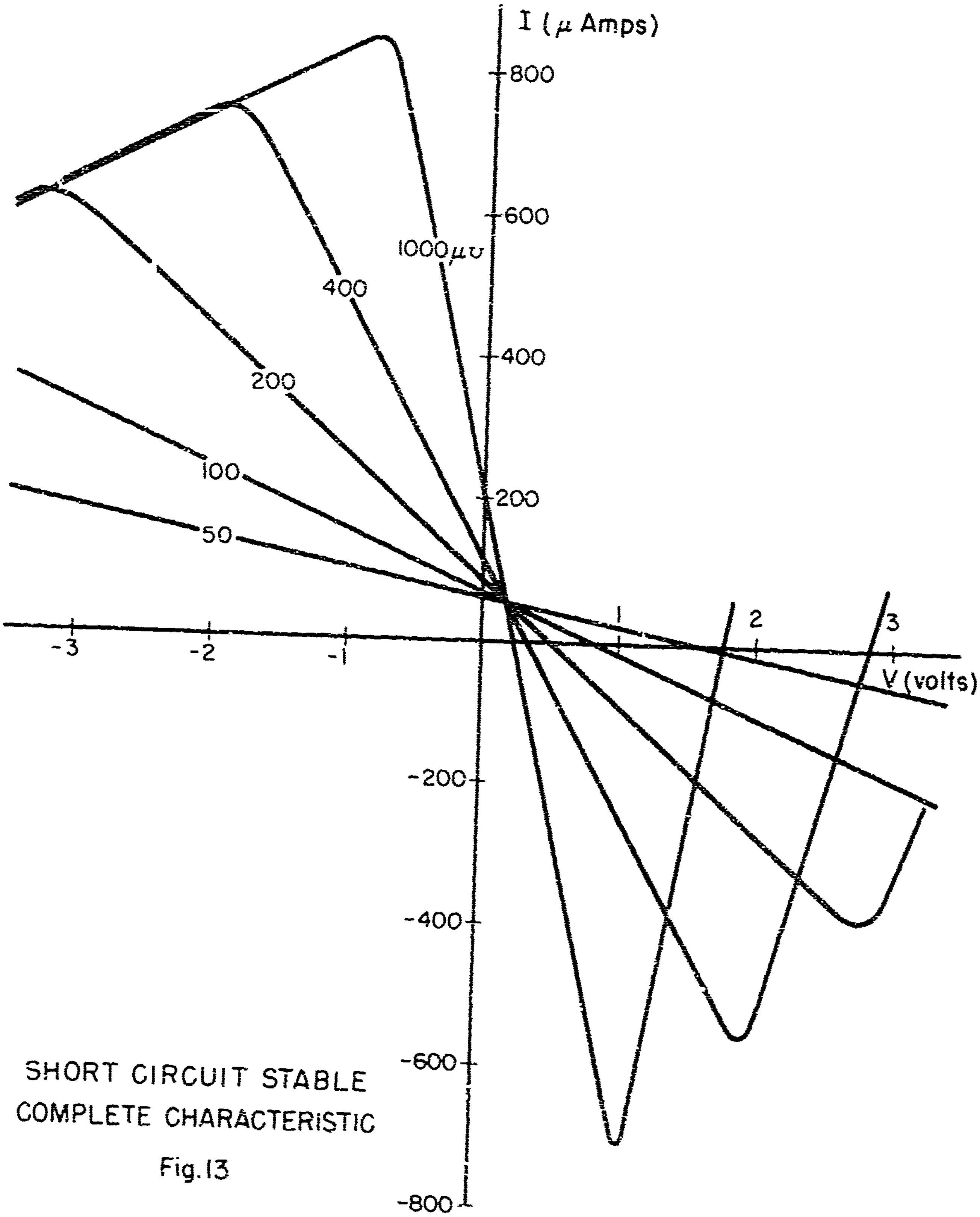
*To obtain this plot the shunt R_m and L_m are replaced with a series R_m and C_m.



SHORT CIRCUIT STABLE
ACTIVE REGION
Fig. 11

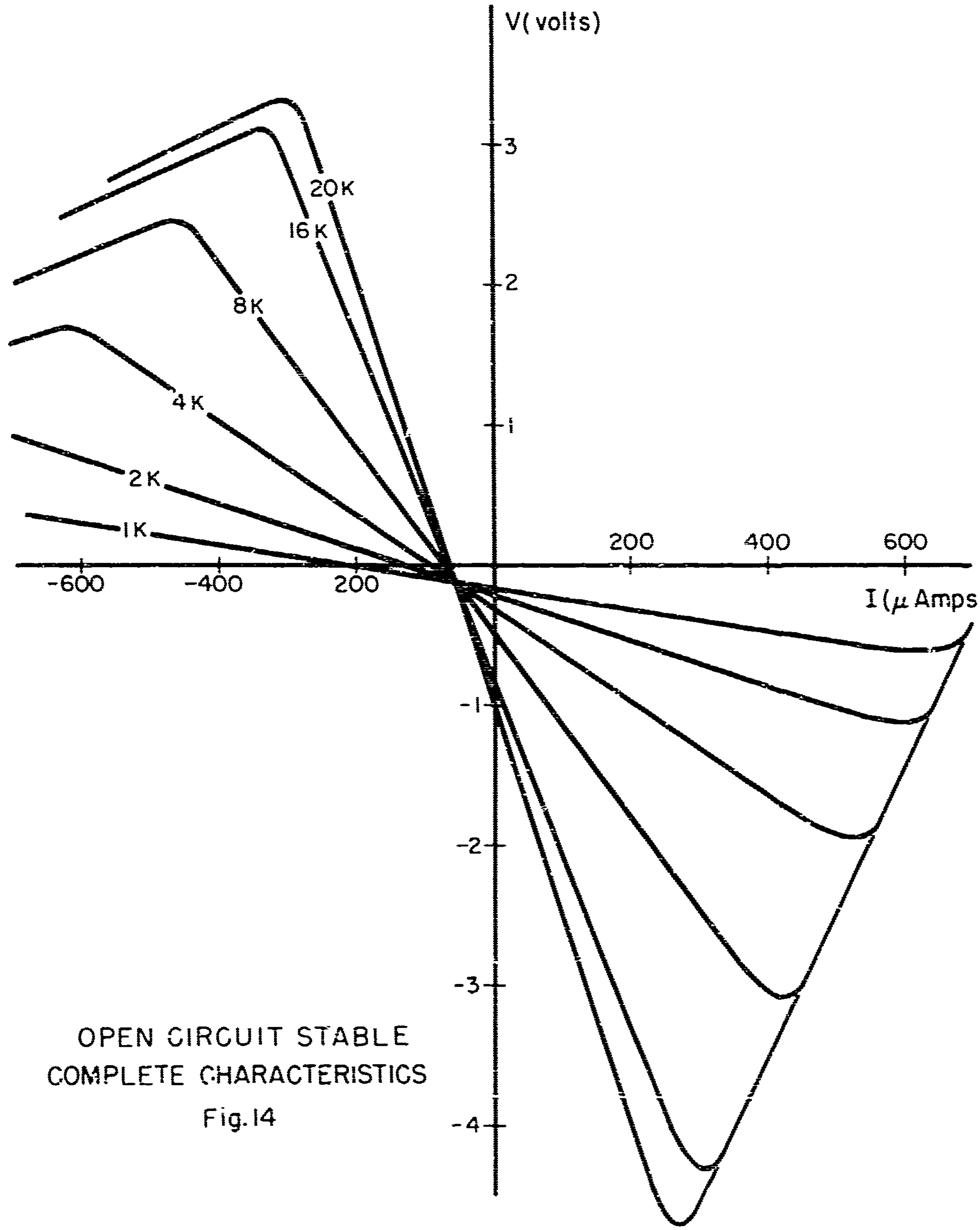


OPEN CIRCUIT STABLE
ACTIVE REGION
Fig. 12

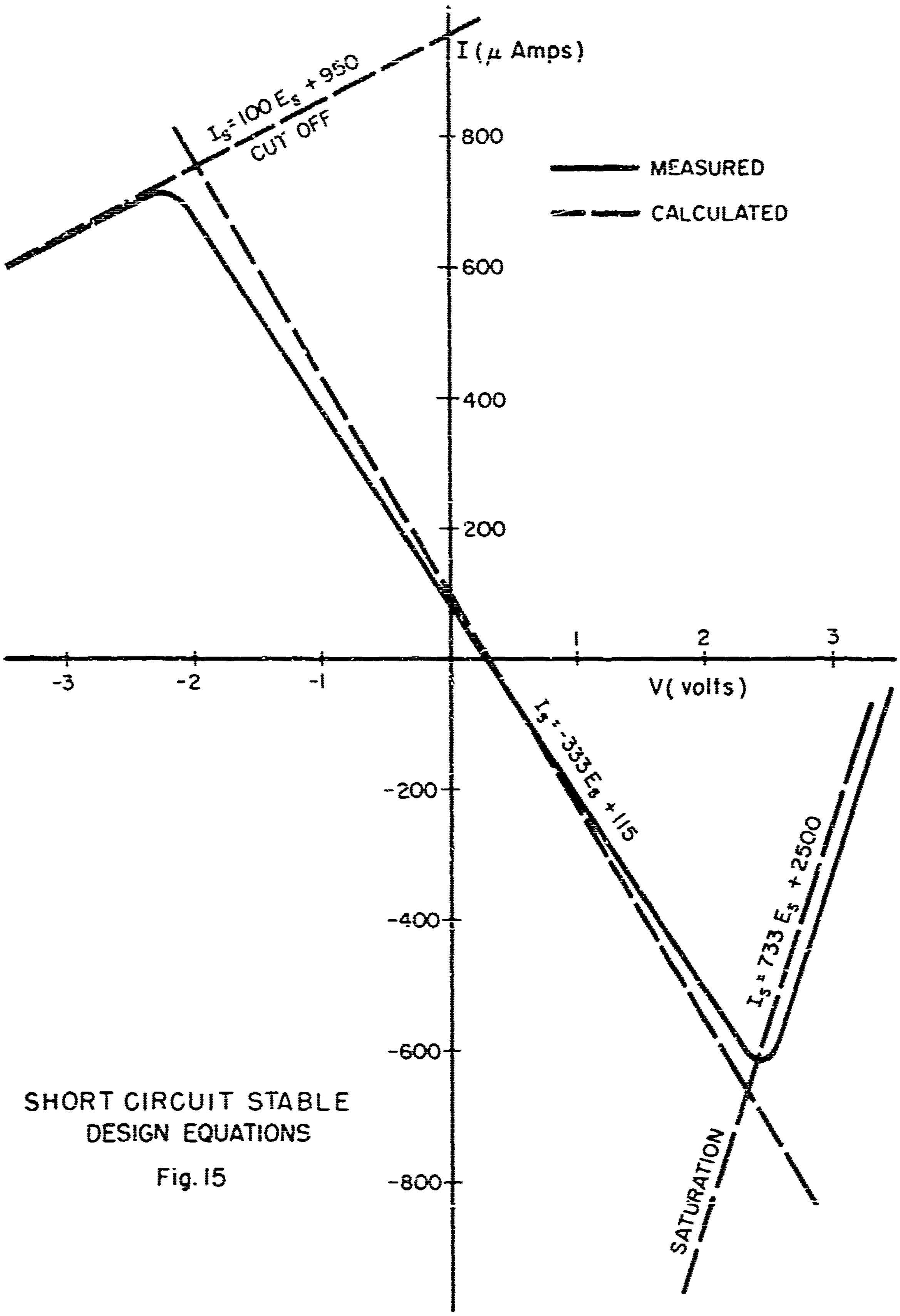


SHORT CIRCUIT STABLE
COMPLETE CHARACTERISTIC

Fig. 13

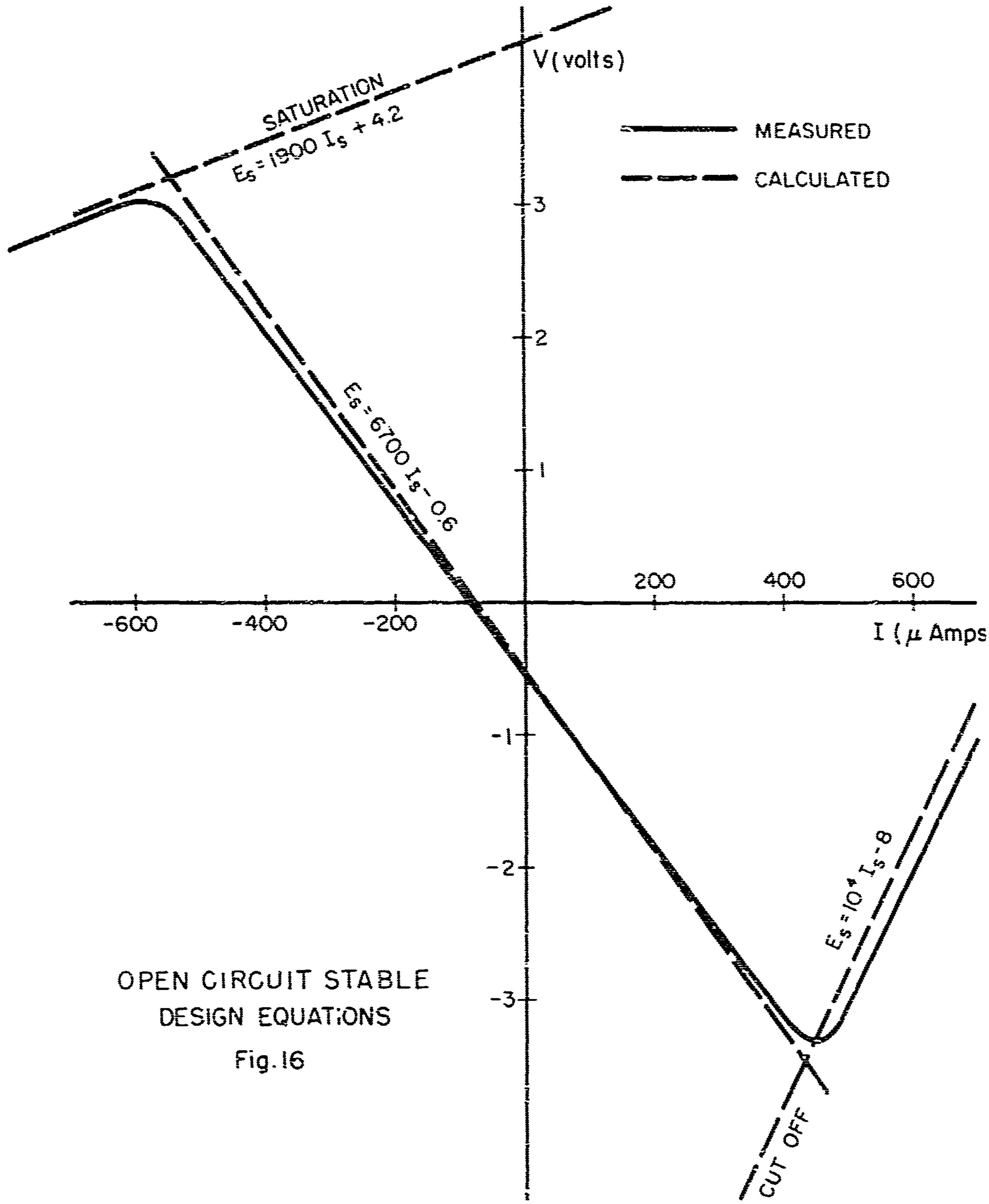


OPEN CIRCUIT STABLE
COMPLETE CHARACTERISTICS
Fig. 14

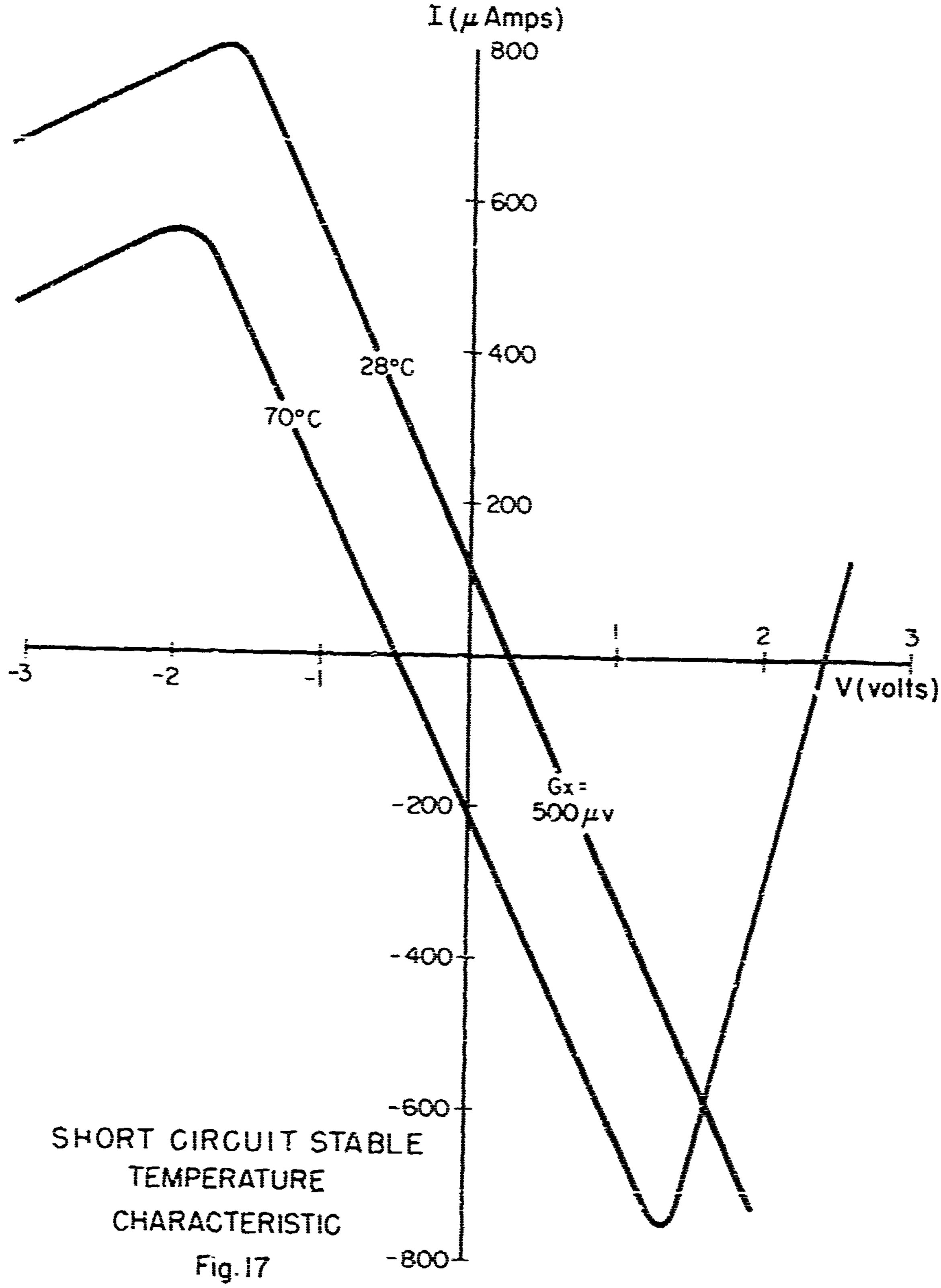


SHORT CIRCUIT STABLE
DESIGN EQUATIONS

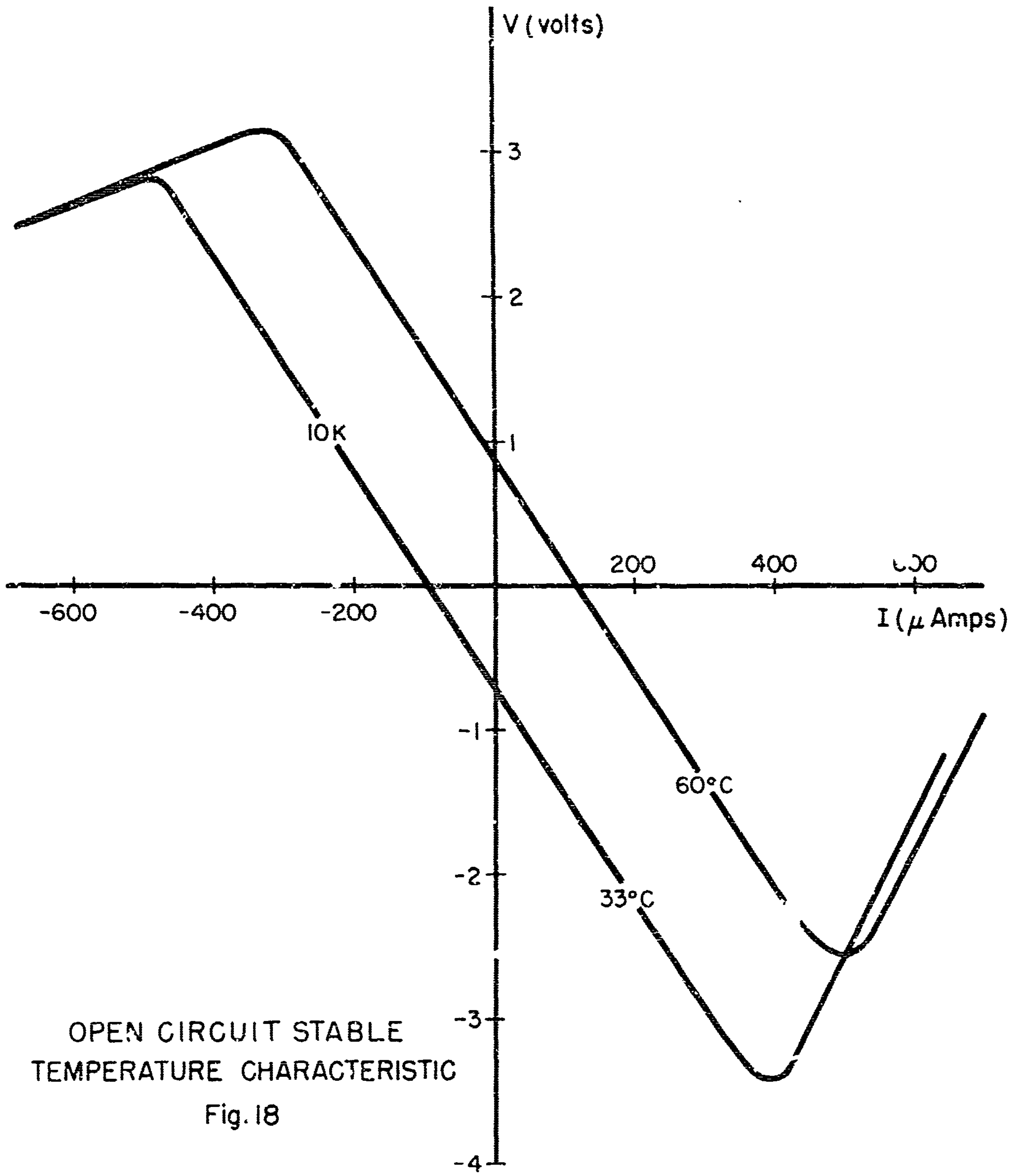
Fig. 15



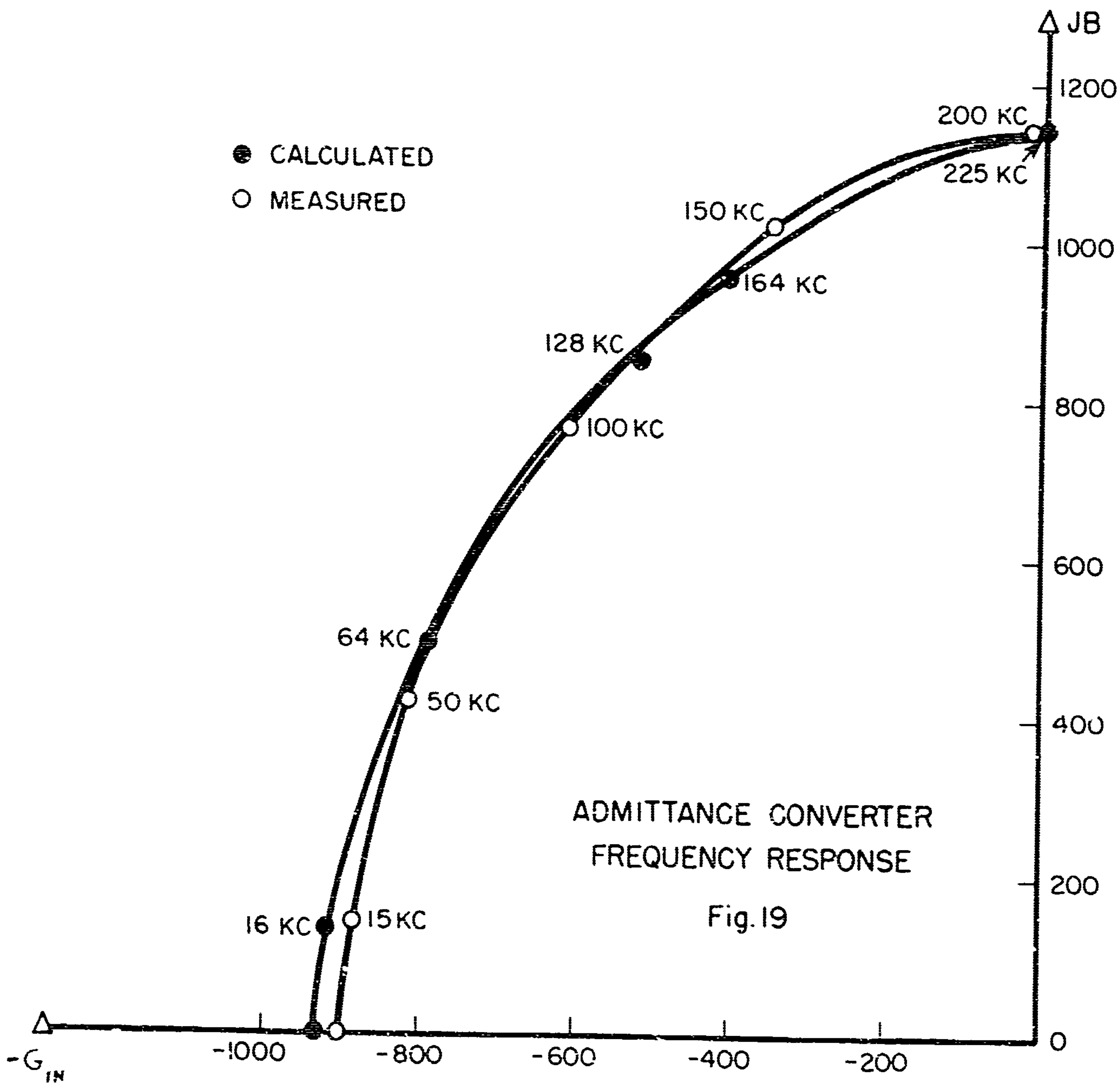
OPEN CIRCUIT STABLE
DESIGN EQUATIONS
Fig. 16



SHORT CIRCUIT STABLE
TEMPERATURE
CHARACTERISTIC
Fig. 17



OPEN CIRCUIT STABLE
TEMPERATURE CHARACTERISTIC
Fig. 18



ADMITTANCE CONVERTER
FREQUENCY RESPONSE

Fig. 19

APPENDIX A

OPEN CIRCUIT STABLE CONVERTER DERIVATION

$$\left.\begin{aligned} F(o) &= \frac{\Delta}{\Delta^\circ} = \frac{G_{c_1}G_{c_2} - \alpha_1\alpha_2G_1G_2}{(G_{c_1} + G_2)(G_{c_2} + G_1)} \\ Y(o) &\approx G_1 + G_{c_2} \end{aligned}\right\}$$

(This is the same as the short circuit converter.)

$$F(\infty) = \frac{\Delta}{\Delta^\circ}\bigg|_{G_1+g_{e_1}} = \frac{G_{c_2}G_{c_1} - \alpha_1\alpha_2G_2g_{e_1}}{(G_{c_1} + G_2)(G_{c_2} + g_{e_1})}$$

$$Y_{in} = \frac{(G_{c_2}G_{c_1} - \alpha_1\alpha_2G_1G_2)(g_{e_1} + G_{c_2})}{(G_{c_2}G_1 - \alpha_1\alpha_2G_2g_{e_1})}$$

$$\approx \frac{(G_{c_2}G_{c_1} - \alpha_1\alpha_2G_1G_2)}{-\alpha_1\alpha_2G_2}, \text{ for } g_{e_1} \gg G_{c_2} \text{ and } G_1 \approx G_2$$

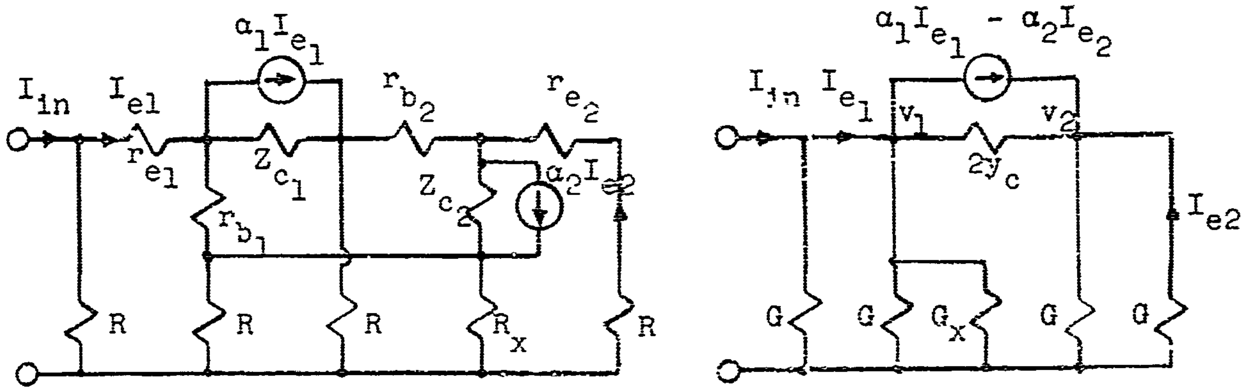
$$\approx G_1 - \frac{(G + G_x)}{\alpha_1\alpha_2G_2}$$

$$Y_{in} \approx G - \frac{(G + G_x)}{\alpha_1\alpha_2} = \frac{G(\alpha_1\alpha_2 - 1) - G_x}{\alpha_1\alpha_2}$$

$$Z_{in} \approx -\alpha_1\alpha_2R_x, \text{ for } G \approx G_x, \text{ and } \alpha_1\alpha_2 \approx 1.$$

APPENDIX B

OPEN CIRCUIT STABLE CONVERTER FREQUENCY RESPONSE



$$I_{e1} = I_{in} - V_1 G \qquad I_{e2} = -v_2 G$$

$$\begin{bmatrix} I_{in}(1-\alpha) \\ \alpha_1 I_{in} \end{bmatrix} = \begin{bmatrix} G(2-\alpha_1) + G_x + 2y_c & -(2y_c - \alpha_2 G) \\ -(2y_c - \alpha_1 G) & G(2-\alpha_2) + 2y_c \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$v_1 = \frac{I_{in}(1-\alpha_1)[G(2-\alpha_2) + 2y_c] + \alpha_1 I_{in}(2y_c - \alpha_2 G)}{\Delta}$$

$$\text{Therefore: } Z_{in} = \frac{(1-\alpha_1)[G(2-\alpha_2) + 2y_c] + \alpha_1(2y_c - \alpha_2 G)}{\Delta}$$

$$\alpha_1 = 1 - pT_1, \quad \alpha_2 \approx 1 - pT_2, \quad y_c = g + pc$$

Substituting the above results in:

$$Z_{in} \approx R_x \left[\frac{-1 + p(2Rc + T_2 + 2T_1)}{1 + p(2KC + K_1 G - T_1 G_x)R_x} \right]$$

The above assumes that:

$$2gK << G_x$$

$$2gR << 1$$

$$K = 4 + R/R_x$$

$$K_1 = (T_1 + T_2)(2 + R/R_x)$$

The following indicates the calculation of ω_o, the frequency when $R_e(Z_{in}) = 0$.

$$Z_{in} = R_x \left[\frac{(-1 + pA')(1 - pB')}{1 - (pB')^2} \right]$$

$$R_e(Z_{in}) = R_x \left[\frac{-1 + \omega^2 A'B'}{1 + (\omega B')^2} \right]$$

Therefore:

$$\omega_o^2 = \frac{1}{A'B'} = \frac{G_x}{(2RC + T_2 + 2T_1)(2KC + K_1 G - T_1 G_x)}$$

The computation of ω_{3db} is as follows:

$$R_e Z_{in}(o) = -R_x$$

$$R_e Z_{in}(\omega_{3db}) = -\frac{R_x}{\sqrt{2}} = R_x \frac{(-1 + \omega^2 A'B')}{1 + (\omega B')^2}$$

$$\omega_{3db} = \frac{.414}{B'(\sqrt{2}\ A'B')} = \frac{.414\omega_o^2}{\sqrt{2} + (B'\omega_o)^2}$$

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ACKNOWLEDGEMENT

The author wishes to express his appreciation for the many helpful suggestions of Mr. M. Joyce. Special thanks is due Mr. G. B. Bush, who suggested the specific circuit and constantly presented many stimulating ideas. It is a pleasure to thank Dr. A. G. Schulz, who provided innumerable constructive criticisms and offered freely of his time. Mrs. D. Cornwell most excellently prepared the complete thesis for reproduction.